

### ABSTRACT

A low loss on-die interconnect structure includes first and second differential signal lines on one of the metal layers of a microelectronic die. One or more traces may also be provided on another metal layer of the die that are non-parallel (e.g.,  
5 orthogonal) to the differential signal lines. Because the traces are non-parallel, they provide a relatively high impedance return path for signals on the differential signal lines. Thus, a signal return path through the opposite differential line predominates for the signals on the differential lines. In one application, the low loss interconnect structure is used within an on-die salphasic clock distribution network.

"Express Mail" mailing label number: EL637138936US

Date of Deposit: June 27, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.